A high-NIR sensitivity SOI-gate lock-in pixel with improved modulation contrast

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Outline

- Background
  - Overview
  - Issues with previous Pixel
- Proposed Pixel Structure
- Simulation Results
  - Potential distribution
  - Parasitic light sensitivity (PLS) and modulation contrast (M.C.)
  - Range resolution
- Summary

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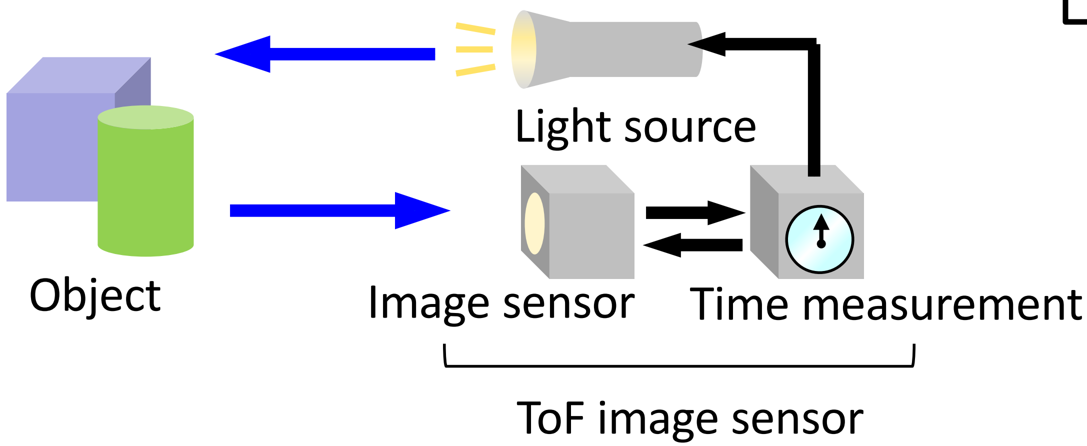
Overview

Time-of-Flight : TOF

Measure the distance to the object from T_{tof}

$$D = \frac{1}{2} c T_{tof}$$

c : velocity of light
T_{tof} : time of flight



Advantages

- High-speed measurements
- No baseline required

Application for outdoor

- Automotive
- Drone

Outdoor long-range measurements

- Strong sunlight

⇨Near-infrared region (NIR) light source

- Long-range measurement

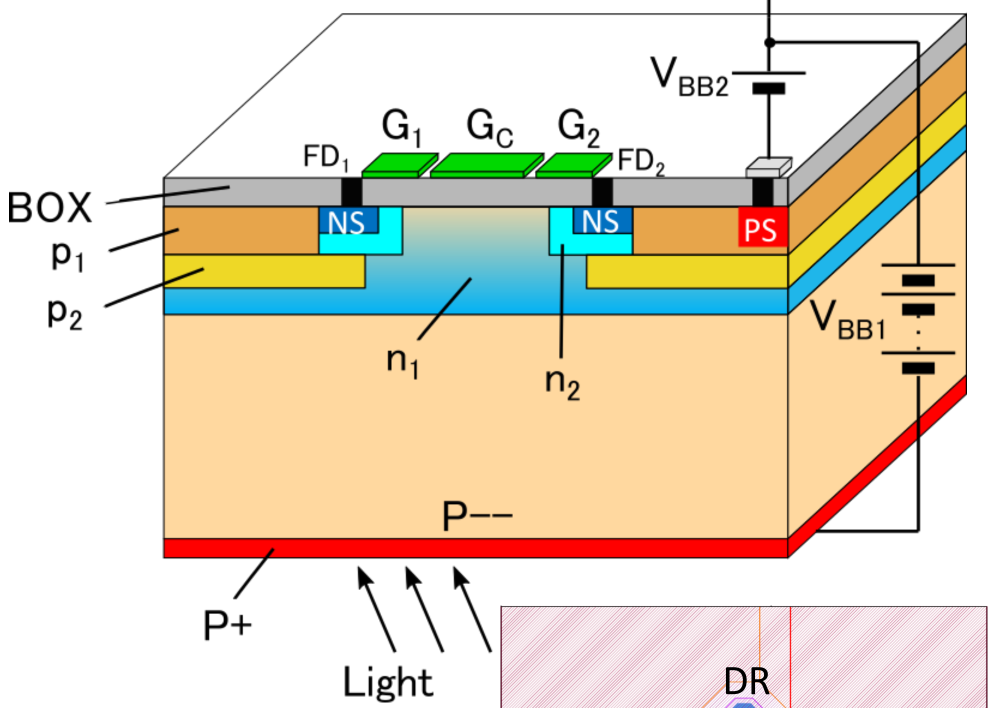
⇨High sensitivity

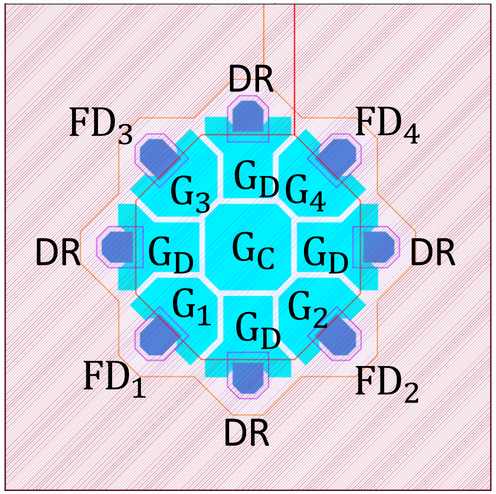
High NIR sensitivity sensors are required

The SOI-based lock-in pixel : Ideal QE@940nm : 96%

The SOI-based lock-in pixel[1]

[1]. S. Lee, K. Yasutomi, et al. Sensors, 20(1).





Pixel size:
18 μm × 18 μm

Features:

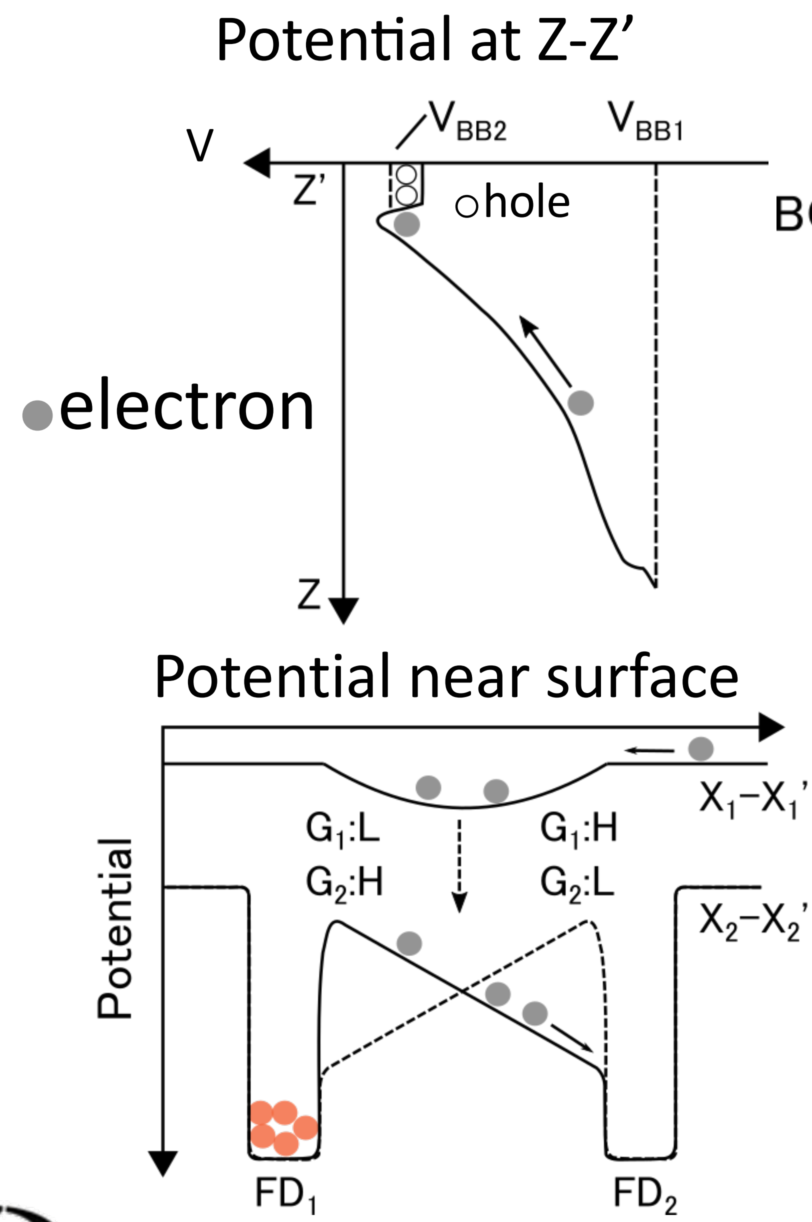
Substrate

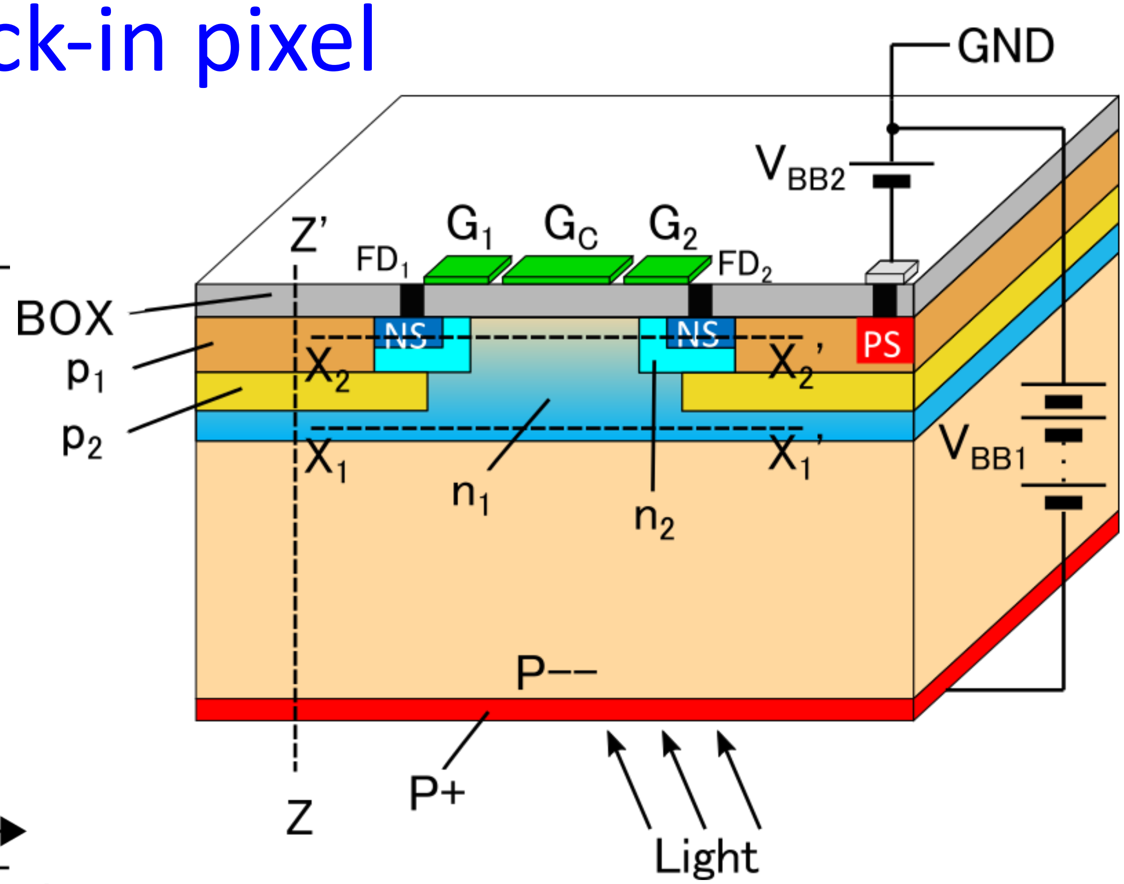
・Thick substrates (=150μm) fully depleted by applying a high reverse bias voltage (>100V)
・High fill factor due to back-side illumination
⇨High QE@940nm

SOI layer

・SOI-gate
⇨High-speed charge modulation
・Multi-tap structure
⇨Long-range measurement and high range resolution

The SOI-based lock-in pixel





n_1 : form buried channel
prevent a punch–though current

n_2 : assist in charge transfer

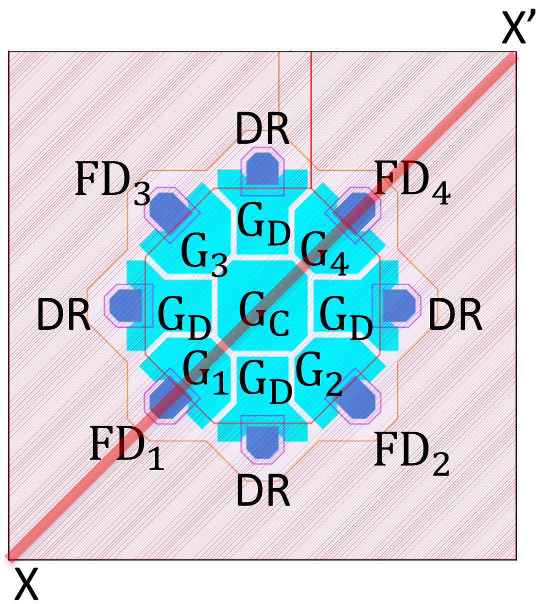
p_1 : fixed surface potential
hole accumulation

p_2 : reduce the parasitic sensitivity

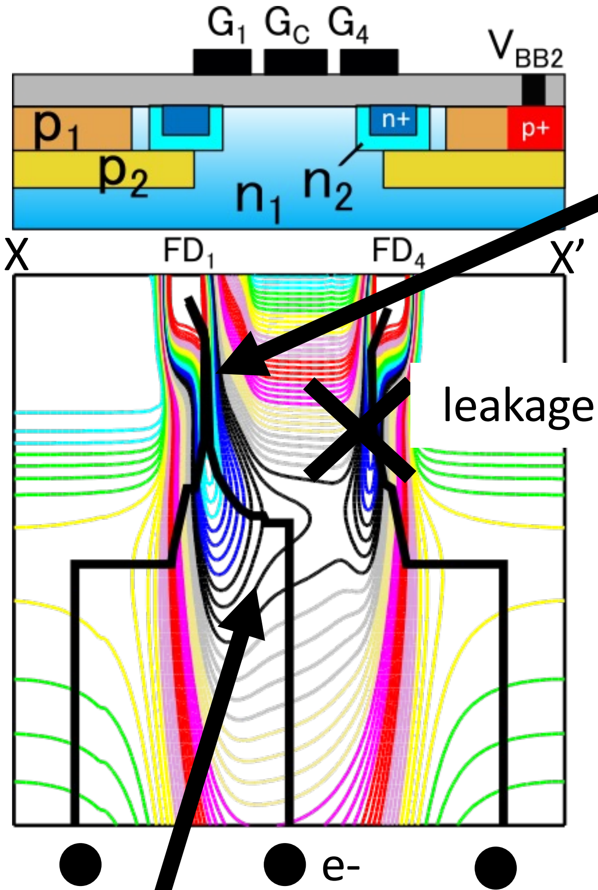
The issue with previous Pixel

Issue : High parasitic light sensitivity (PLS >10%)

Previous pixel layout



Voltage condition
G1 : -4V
GC,GD,G2～G4 : -7V



High n_2 concentration is required to connect buried channel and FD

⇩

The connection still exists when the modulation gate is off.
⇨High PLS
⇨Degradation of range resolution and internal QE

Buried channel by n_1

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Proposed Pixel Structure

Improvement points:

①The shallow channel (n_1⇨ n_3)⇨improvement of potential controllability

②The additional gates⇨Enhance the lateral electric field

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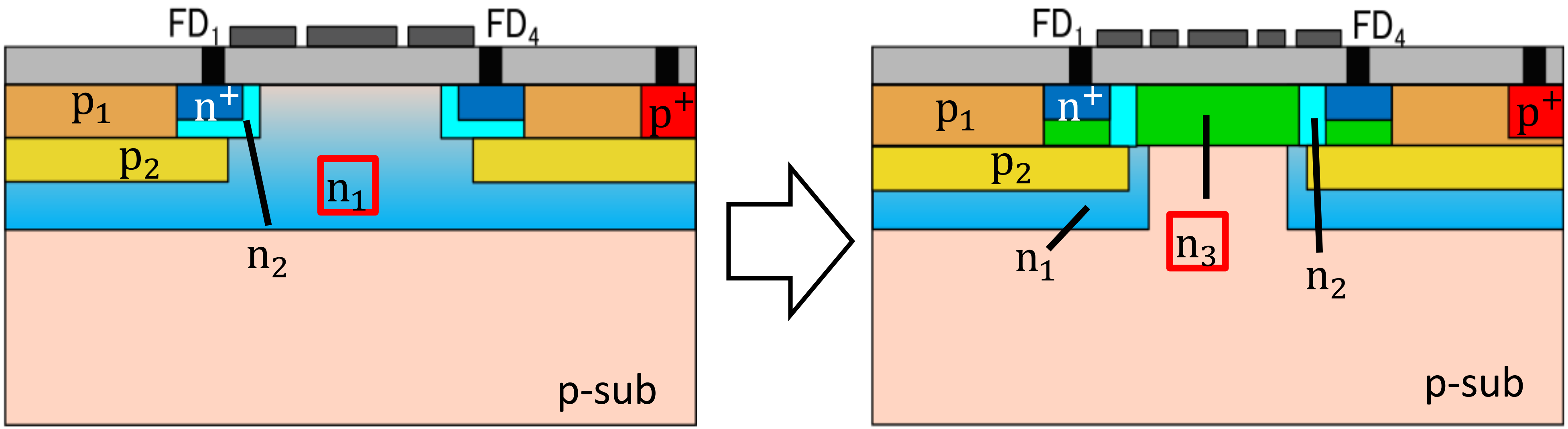

- Deeply buried channel by n_1
- Insufficient potential barrier by p_2 due to high n_2 concentration

- Shallower buried channel by n_3
- Reduction of n_2 concentration (1/3 of previous structure)

⇨Form sufficient barrier to prevent PLS

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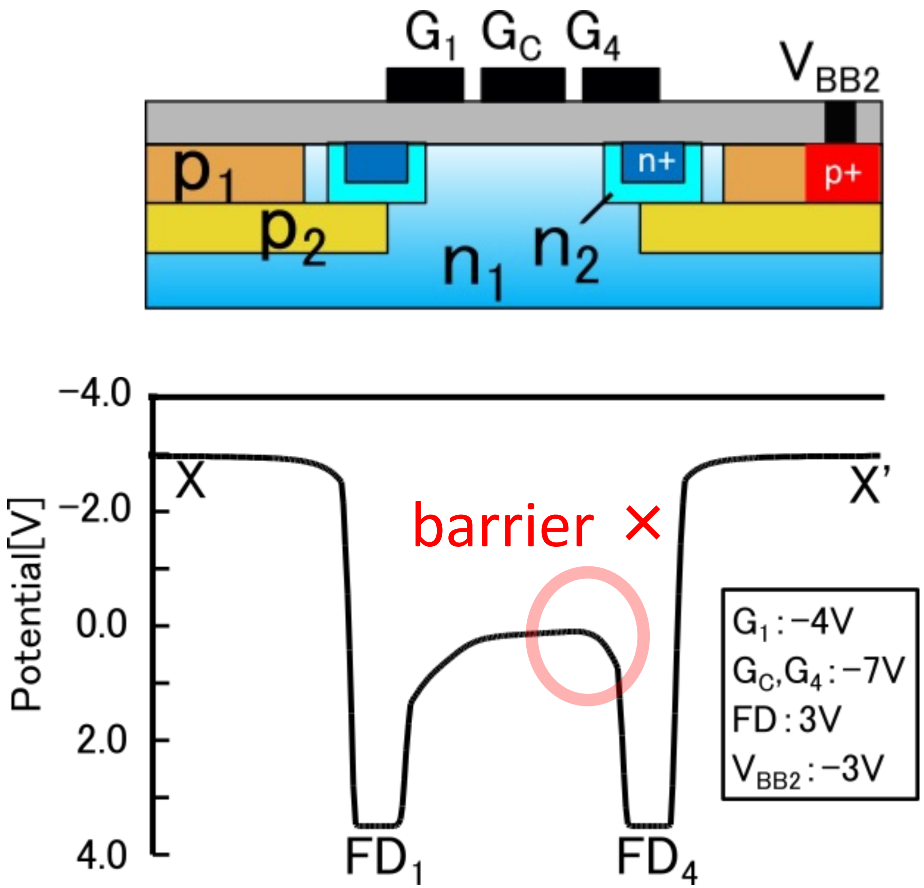

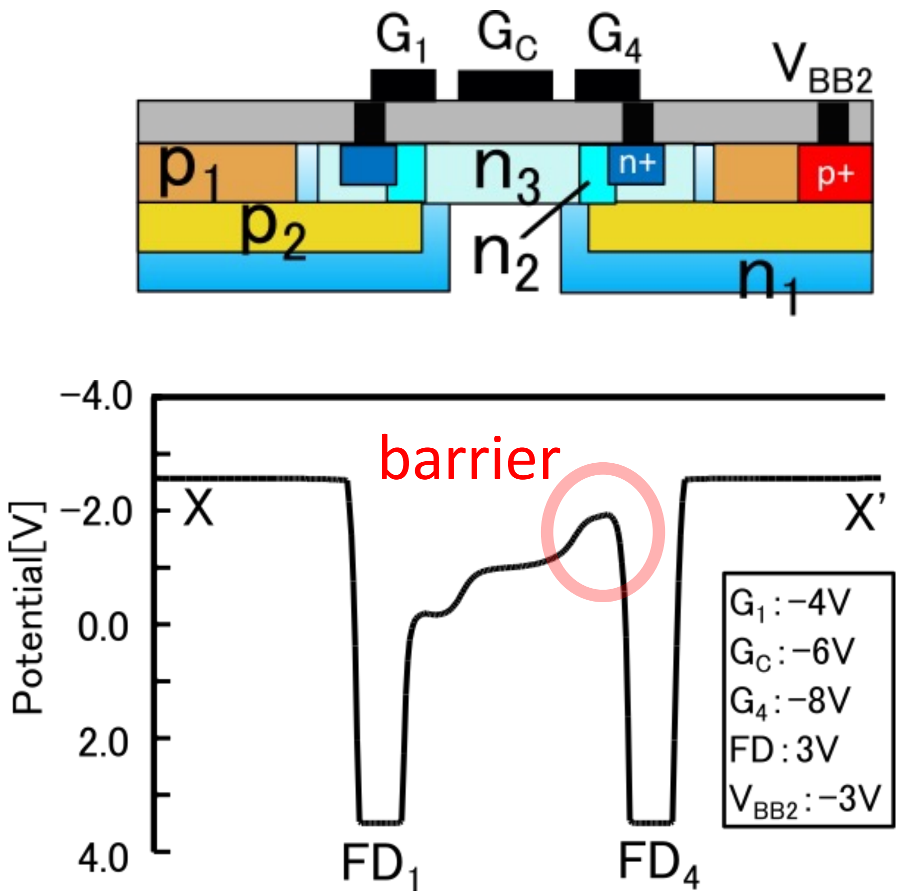

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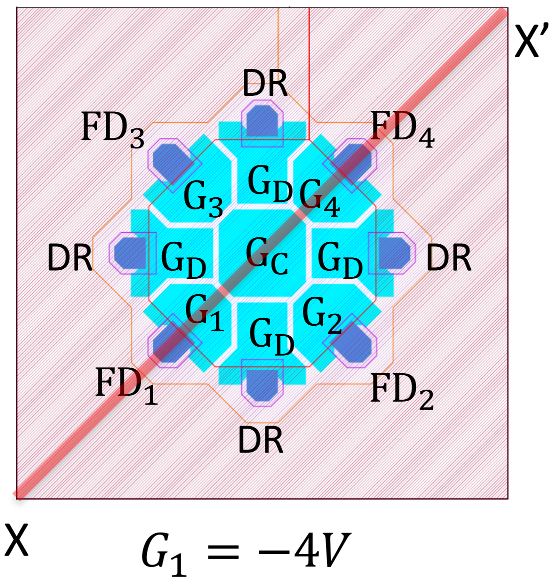
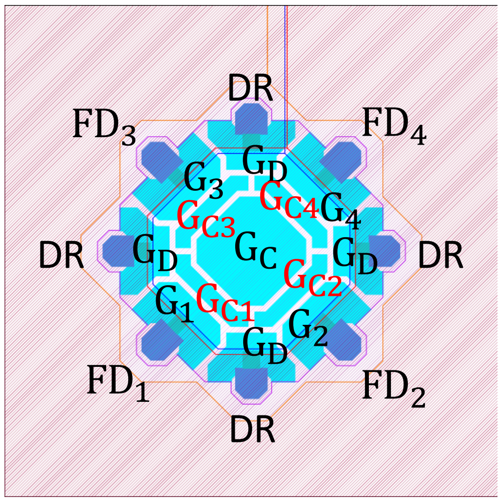
previous pixel



$$G_1 = -4V$$
$$G_C = -6V$$
$$G_2 \sim G_4, DR = -8V$$
$$FD = 3V$$
$$V_{BB2} = -3V$$

Proposed pixel



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$$G_{C1}, G_C = -6V$$
$$G_{C2} \sim G_{C4}, G_2 \sim G_4, DR = -8V$$
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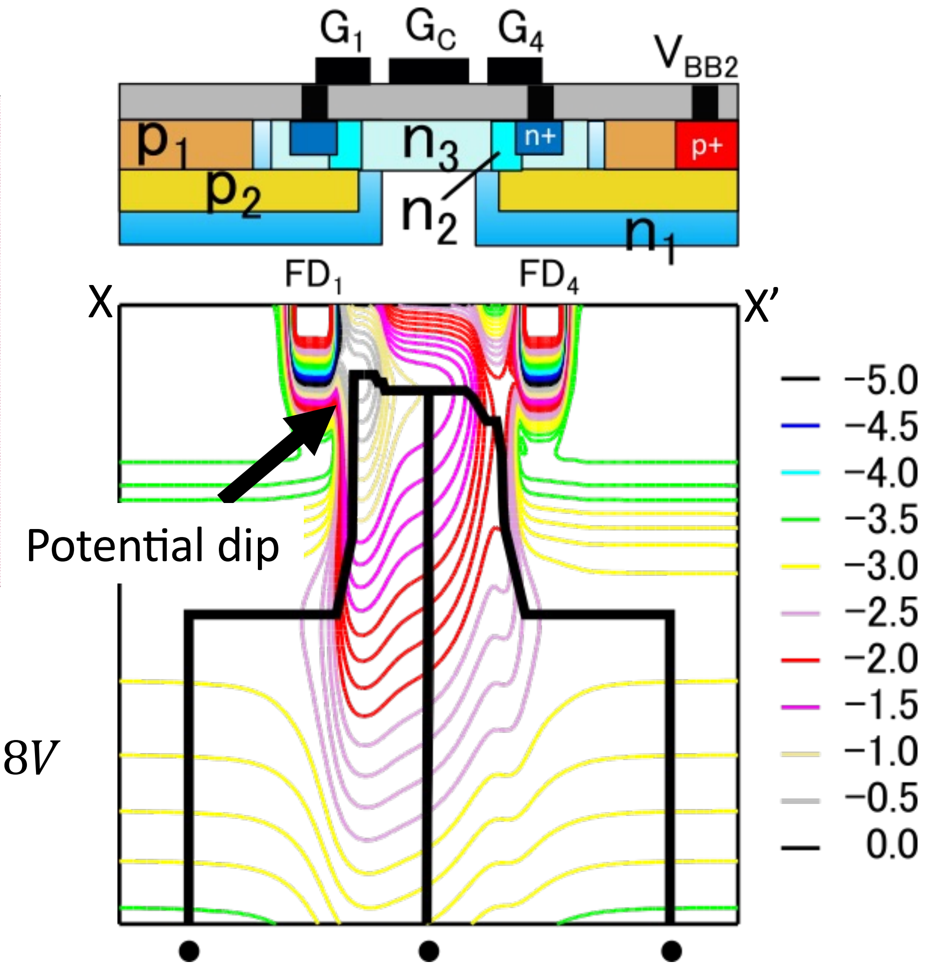

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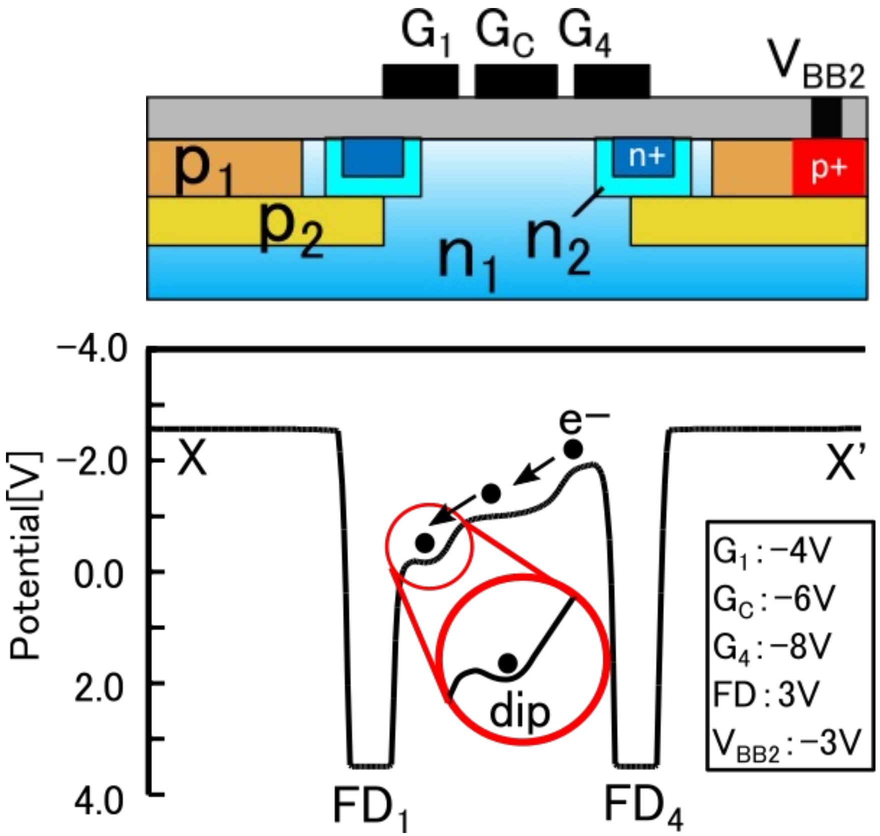

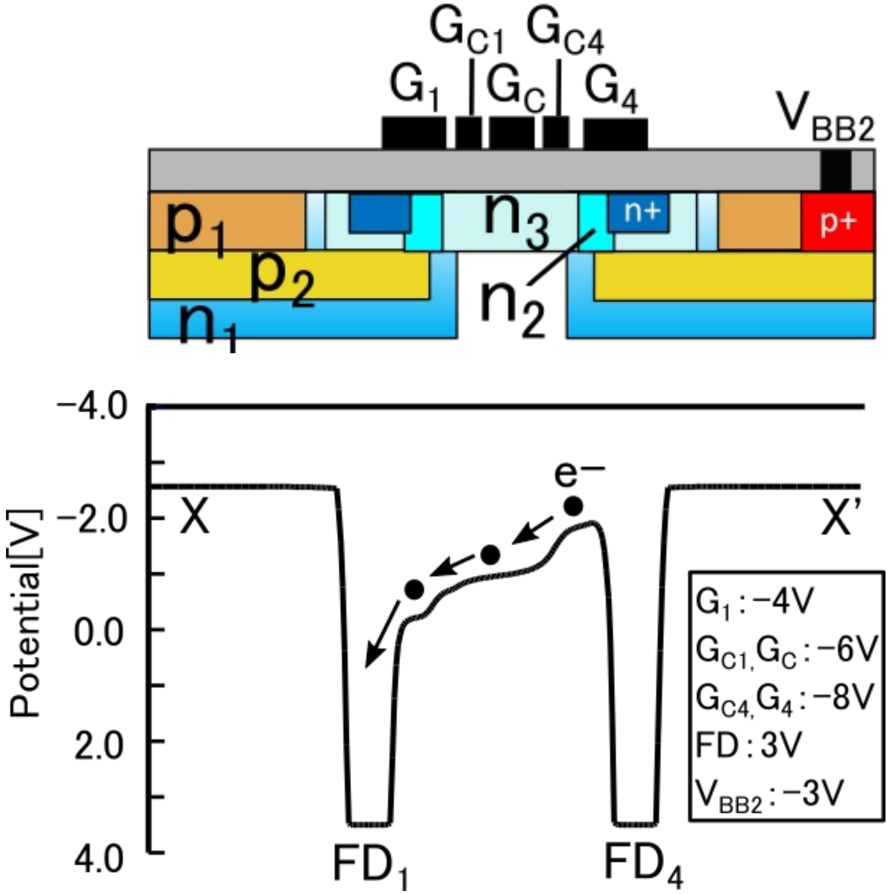

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Parasitic light sensitivity (PLS) modulation contrast (MC)

✓ **Simulation conditions**

Light

- Light wavelength **λ : 940nm**
- Light power density P_i **: 271E-6[W/cm²]**
- Light pulse width : **25ns**
- A constant light with normal incidence was irradiated to the whole area of the backside.

Voltage

- Only G_1 turned on and G_2-G_4 (GC_2-GC_4) and GD turned off.

Previous : G_1=-4V, G_2-G_4=GC=-7V

Proposed : G_1=-4V, GC_1=GC=-6V, GC_2-GC_4=G_2-G_4=-8V

✓ **Definitions**

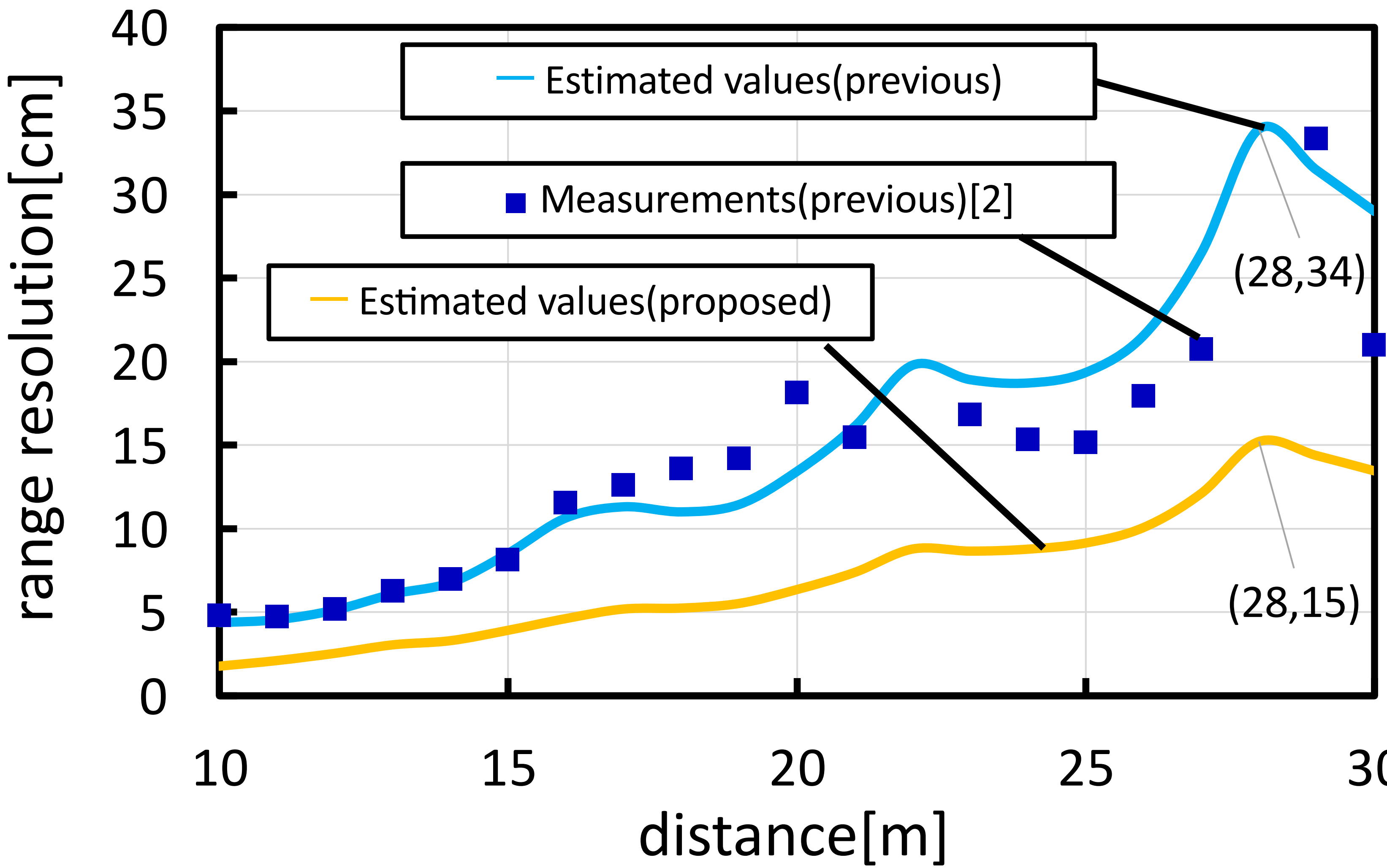
$$\mathrm{PLS}[\%] = 100\times \frac{I_{FD}OFF}{\sum I_{FD1}\sim I_{FD4}}$$

$$\mathrm{MC}[\%] = 100\times \frac{I_{FD}ON}{\sum I_{FD1}\sim I_{FD4}}$$

	Previous	Proposed
PLS[%]	13.3	0.03
MC[%]	59.7	99.9

- PLS is reduced to less than 1/400 of previous pixel (≒0%)
- MC improves to almost 100%.

Estimated improvement of range resolution



[2]. Naoki TAKADA, Keita YASUTOMI, et al. EI2022

Summary

- We proposed a high-NIR sensitivity SOI-gate lock-in pixel with improved modulation contrast.
  - Reduction of parasitic light sensitivity (13.7%⇨0.13%)
  - Improvements of modulation contrast (58.7%⇨99.6%) and range resolution (28cm⇨15cm@28m)
- Future outlook on research
  - Evaluation of protype chip in July 2023